Design and realization of sub 100nm gate length HEMTs

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The demand for higher bit-rate communication is rapidly growing. 40Gbit/s system has been recently developed [1] and intensive research on 80Gbit/s and 160Gbit/s is being done. One way to obtain these bit-rates is the use of InP-based HEMTs and the reduction of gate length to nanometer dimension. With InP-based HEMTs, it is possible to reach f_T higher than 300GHz [2] and f_{max} up to 600GHz [3]. To obtain high f_T and f_{max} devices, the important point is the layer structure and the aspect ratio. Figure 1 illustrates typical layer structure for 100nm gate length lattice-matched HEMT. To improve frequency performance, optimized layer structure for 50nm gate length HEMT was designed. This structure has to be a trade-off between a high aspect ratio, and the necessity to take care at several physical limitations, as the tunneling current across the Schottky barrier or the increase of the quantum energy levels in the quantum well. A 2D Monte Carlo model was used to accurately simulate 50nm gate device [4]. Influence of doping level in the δ-doped layer, recess length, gate-to-channel separation and Indium content was studied. The optimized structure for a 50 nm gate length HEMT is presented in Figure 2. Important parameters are a high Indium content of 0.65 in the channel to improve carrier transport properties, and Aluminum content of 0.65 in the Schottky layer to limit tunneling effect.

Standard and optimized structures were realized by molecular beam epitaxy. Nanometer gate length HEMTs were processed on the lattice matched layer structure designed for the 100nm gate device (figure 1) and the optimized structure (figure 2). First the mesa isolation was defined by H_3PO_4:H_2O_2:H_2O solution. Ohmic contact Ni/Ge/Au/Ni/Au was evaporated followed by 1 minute rapid thermal annealing at 310 °C. Typical ohmic contact resistance of 0.15 to 0.2 Ω.mm was measured. The T-shaped gate was defined using a bilayer resist PMMA/P(MMA-MAA) scheme and a 100keV Leica EBPG-5HM machine. InGaAs cap layer was selectively removed using Succinic Acid solution. Finally Ti/Pt/Au gate was evaporated as well as the bonding pads (figure 4).

S-parameter measurements were performed up to 50GHz for both devices and small signal equivalent circuit was extracted (table 1). Figure 3 shows the extrinsic $|H_{21}|^2$ and unilateral gain U versus frequency for the HEMTs realized on optimized structure. –6dB/octave extrapolation give a f_T of 240GHz and a f_{max} of about 470GHz. These results have to be compared with those of standard LM-HEMT reported in table 1. For the standard LM-HEMT, we obtained a maximum cutoff frequency f_T of 270 GHz, but f_{max} is only 260 GHz. In case of the optimized HEMT, a slightly lower f_T is obtained that can be explained by a higher gate length (Electron beam microscopy observations gave a gate length of 60nm for the standard device and 70nm for the optimized one), and poorer access resistances [5]. However, the maximum oscillation frequency f_{max} for the optimized HEMT, 470 GHz, exceeds largely the 260 GHz value obtained with the standard structure. This high f_{max} is due to the improved ratio G_m/G_d and C_{gs}/C_{gd} obtained with the optimized layer, and is related to a reduction of short channel effects. This value can be further improved by reducing the Rs and Rd access resistances. This last result demonstrates the potential of our optimized structure for high frequency performance, and predicts f_T and f_{max} respectively beyond 300GHz and 600GHz for a sub-50nm gate length HEMT using the same scaling down rules.

References

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Cap Layer	10nm	GaInAs ($5x10^{18}$ at/cm^3)
Barrier	12nm	AlInAs (n.i.d.) 52% Al
Spacer	5nm	AlInAs (n.i.d.) 52% Al
Channel	20nm	GaInAs (n.i.d.) 53% In
Buffer	200nm	AlInAs (n.i.d.)
S.I. InP Substrate		

δ-doped layer $5x10^{12}$ Si/cm^2

Fig 1 : Standard layer structure for 100nm HEMT

Cap Layer	10nm	GaInAs ($5x10^{18}$ at/cm^3)
Barrier	**8**nm	AlInAs (n.i.d.) **65**% Al
Spacer	**3.5**nm	AlInAs (n.i.d.) **65**% Al
Channel	**10**nm	GaInAs (n.i.d.) **65**% In
Buffer	200nm	AlInAs (n.i.d.)
S.I. InP Substrate		

δ-doped layer **6**$x10^{12}$ Si/cm^2

Fig 2 : Optimized layer structure for 50nm HEMT

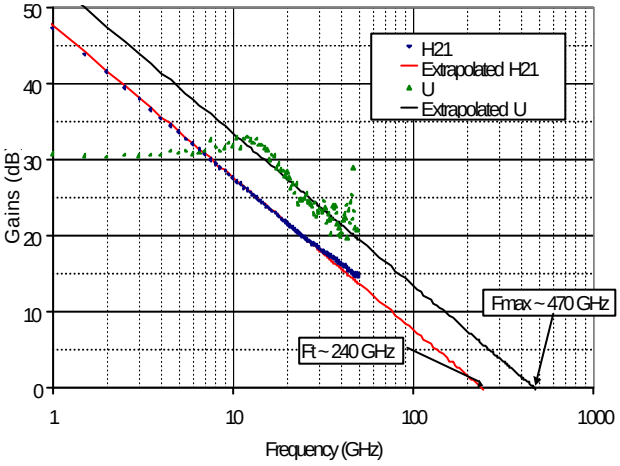

Fig 3 : Performances of 70nm x 100µm HEMT processed on the optimized layer structure, at Vds=1V, and Vgs=0.1V.

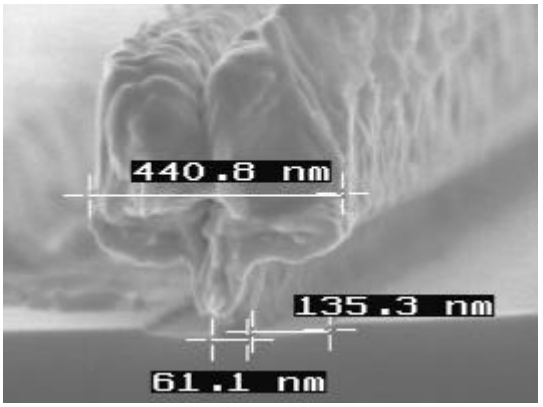

Fig 4 : T-shaped gate processed with a bilayer resists of HEMT standard layer structure

	Gm (mS/mm)	Gd (mS/mm)	Gm/Gd	Cgs (fF/mm)	Cgd (fF/mm)	Cgs/Cgd	Fc (GHz)	Ft (GHz)	Fmax (GHz)
60nm HEMT, on a std. Layer	**1180**	175	**6.7**	440	86	**5.1**	425	270	**260**
70nm HEMT, on a optimized layer	**1550**	83	**18.7**	735	94	**7.8**	335	240	**470**

Table 1 : Comparison for the small signal value of the standard layer and the optimized layer structure, At Vds = 1V, and Vgs for the maximum of Gm .